Remarks

Applicants respectfully request reconsideration of this application as amended. No claims have been amended. No claims have been cancelled. Therefore, claims 48-53 and 56-76 are presented for examination.

Claims 48-53 and 56-76 stand rejected under 35 U.S.C. §102(e) as being anticipated by Okada et al. (JP 05290334 A). Applicants submit that the present claims are patentable over Okada.

Okada discloses a first memory means used to store a low order digit of count data and a second, non-volatile memory means used to store a high order digit of the count data. The first memory means is updated during every renewal of the low order digit of count data. Whenever carry occurs in a low order digit the second memory means is updated. See Okada at [0013].

Claim 48 of the present application recites:

> A method comprising:
> maintaining a first value for a first counter based on a content of a volatile memory as a first component of a monotonic count;
> maintaining a second value for a second counter based on a content of a non-volatile memory as a second component of a monotonic count; and
>
> controlling updates to the first value for the first counter and to the second value for the second counter at control logic by updating the first value for the first counter in response to the reading of the monotonic count.

Applicants submit that nowhere in Okada is there disclosed updating a first value for a first counter in response to the reading of a count. Instead, Okada discloses updating a first memory means during every renewal of a low order digit of count data. Nevertheless, there is no disclosure of the low order digit or the first memory means being updated in response to reading the count data. The Examiner asserts that it is:

> [inherent to the system as to display the reading, the system has to read the monotonic count in between the first update and the next update of the first counter and thus the first value of the counter is updated in response to the reading of the monotonic count].

See Office Action at page 3, paragraph 5, lines 10-12.

Applicants do not to understand how displaying a count reading between a first update and a next update makes inherent updating a count value in response to reading a count. Because a count may be read before and after it is updated does not suggest that a count value is updated in response to the count being read. Thus, claim 1 is patentable over Okada since Okada does not disclose updating a first value for a first counter in response to the reading of a count.

Claims 49-53 depend from claim 48 and include additional features. Therefore, claims 49-53 are also patentable over Okada.

Claim 56 recites:

> A method comprising:
> powering on a monotonic counter, the monotonic counter at least partially basing a count value on a content of a volatile memory utilized for lesser significant bits of the count value and a non-volatile memory utilized for higher significant bits of the count value; and
> updating the count value for the monotonic counter by a first value on the powering on condition.

Applicants submit that nowhere in Okada is there disclosed updating a count value upon a powering on condition. In fact, Okada does not disclose a powering on condition. Accordingly, claim 56 is patentable over Okada. Because claim 57 depends from claim 56 and includes additional features, claim 57 is also patentable over Okada.

Claim 58 recites:

> An apparatus comprising:
> a volatile counter to maintain lesser significant bits of monotonic count;
> a non-volatile counter to maintain higher significant bits of the monotonic count based on a content of a non-volatile memory; and

control logic to control updating the first and second counters by updating the first counter when the monotonic count is read.

For the reasons described above with respect to claim 48, claim 58 is patentable over Okada. Claims 59-63 depend from claim 58 and include additional features. Thus, claims 59-63 are also patentable over Okada.

Claim 64 recites:

An apparatus comprising:
a volatile memory to maintain a first value for lesser significant bits of a count value for a first counter;
a non-volatile memory to maintain a second value for higher significant bits of the count value for a second counter; and
circuitry to maintain a monotonic count value, and to update the count value by a number in response to a read of the count value for the monotonic counter.

For the reasons described above with respect to claim 48, claim 64 is patentable over Okada. Since claims 65 and 66 depend from claim 64 and include additional features, claims 65 and 66 are also patentable over Okada.

Claim 67 recites:

An apparatus comprising:
a volatile memory to maintain a first value for a first counter;
a non-volatile memory to maintain a second value for a second counter; and
circuitry to maintain a count value for a monotonic counter, the circuitry to base the count value at least partially on the first value for lesser significant bits of the count value and the second value for higher significant bits of the count value, and to update the count value by a number in response to a powering on condition for the circuitry.

For the reasons described above with respect to claim 56, claim 67 is patentable over Okada. Because claims 68 and 69 depend from claim 67 and include additional features, claims 68 and 69 are also patentable over Okada.

Claim 70 recites:

An apparatus comprising:
one or more registers to store a first value;

a first adder to maintain the first value;

a flash memory to store a portion of bits used for a monotonic count;

one or more registers to store a second value;

a second adder to maintain the second value based on one or more programmed locations in the flash memory; and

a control engine to control the flash memory and the first and second adders, the first value used to determine lower significant bits of the monotonic count and the second value used to determine higher significant bits of the monotonic count, the lesser significant bits being volatile while higher significant bits being non-volatile.

Applicants submit that nowhere in Okada is there disclosed a second adder to maintain the second value based on one or more programmed locations in the flash memory. Therefore, claim 60 is patentable over Okada. Because claims 71 and 72 depend from claim 70 and include additional features, claims 71 and 72 are also patentable over Okada.

Applicants respectfully submit that the rejections have been overcome and that the claims are in condition for allowance. Accordingly, applicants respectfully request the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Applicants respectfully petition for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17(a) for such an extension.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: July 12, 2004

Mark L. Watson
Reg. No. 46,322

12400 Wilshire Boulevard
7th Floor
Los Angeles, California 90025-1026
(303) 740-1980